WHAT IS CLAIMED IS:

1. An integrated circuit comprising a differential impedance termination circuit, the differential impedance termination circuit comprising:

first resistors coupled in series; and

a first transistor coupled in series with the first resistors; and

a first memory coupled to a gate of the first transistor that is programmed to effect an impedance of the impedance termination circuit,

the impedance termination circuit being coupled between first and second differential pins of the integrated circuit.

2. The integrated circuit according to claim 1 wherein the integrated circuit is a field programmable gate array.

3. The integrated circuit according to claim 1 wherein the integrated circuit is an application specific integrated circuit.

4. The integrated circuit according to claim 1 further comprising:

a second transistor;

a second memory coupled to a gate of the second transistor that is programmed to effect the impedance of the impedance termination circuit; and

a second resistor coupled in series with the second transistor, the second resistors and the second transistor being coupled in parallel with at least one of the first resistors when the second transistor is ON.

5. The integrated circuit according to claim 4 further comprising:

a third transistor;

a third memory coupled to a gate of the third transistor that is programmed to effect the impedance of the impedance termination circuit; and

a third resistor coupled in series with the third transistor, the third resistor and the third transistor being coupled in parallel with at least one of the first resistors when the third transistor is ON.

6. The integrated circuit according to claim 4 further comprising:

a third transistor coupled in parallel with the second resistor; and

a third memory coupled to a gate of the third transistor.

7. The integrated circuit according to claim 1 further comprising:

a second transistor coupled in parallel with the first transistor; and

a second memory coupled to a gate of the second transistor that is programmed to effect an impedance of the impedance termination circuit.

8. The integrated circuit according to claim 1 further comprising:

a second transistor coupled in parallel with one or more of the first resistors;

a third transistor coupled in parallel with the second transistor;

a second memory coupled to a gate of the second transistor; and

a third memory coupled to a gate of the third transistor.

9. The integrated circuit according to claim 1 further comprising:

a second transistor coupled in parallel with one or more of the first resistors and the first transistor;

a second memory coupled to a gate of the second transistor that is programmed to effect an impedance of the impedance termination circuit;

second resistors coupled in series with the second transistor;

a third transistor coupled in parallel with one or more of the second resistors; and

a third memory coupled to a gate of the third transistor.

10. A method for providing selectable termination impedance across differential pins on an integrated circuit, the method comprising:

storing a voltage in a first memory;

providing the voltage stored in the first memory to a gate of a first transistor;

conducting current through first resistors when the first transistor is ON; and

blocking current through the first resistors when the first transistor is OFF.

11. The method as defined in claim 10 further comprising:

storing a voltage in a second memory; and

providing the voltage stored in the second memory to a gate a second transistor that is coupled in parallel with the first transistor.

12. The method as defined in claim 11 wherein the second transistor is coupled in parallel with at least two of the first resistors and the first transistor.

13. The method as defined in claim 10 further comprising:

storing a voltage in a second memory;

providing the voltage stored in the second memory to a gate of a second transistor that is coupled in parallel with the first transistor;

conducting current through second resistors coupled in series with the second transistor when the second transistor is ON; and

blocking current through the second resistors when the second transistor is OFF.

14. The method as defined in claim 13 further comprising:

storing a voltage in a third memory;

providing the voltage stored in the third memory to a gate of a third transistor that is coupled in parallel with a first one of the second resistors.

15. The method as defined in claim 14 further comprising:

storing a voltage in a fourth memory;

providing the voltage stored in the fourth memory to a gate of a fourth transistor that is coupled in parallel with a second one of the second resistors.

16. The method as defined in claim 10 further comprising:

storing a voltage in a second memory; and

providing the voltage stored in the second memory to a gate of a second transistor that is coupled in parallel with one or more of the first resistors.

17. The method as defined in claim 16 further comprising:

storing a voltage in a third memory; and

providing the voltage stored in the third memory to a gate of a third transistor that is coupled in parallel with one or more of the first resistors.

18. The method as defined in claim 10 wherein the integrated circuit is a programmable logic device.

19. The method as defined in claim 10 wherein the integrated circuit is an ASIC.